042390.P3991

Patent Application

#21
1/23/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:
Dunning et al.

Serial No.: 08/766,895
Filed: December 13, 1996

For: METHOD AND APPARATUS FOR ROUTING ENCODED SIGNALS THROUGH A NETWORK

Date: October 12, 2001

Art Unit: 2712

Examiner: H. Vu

HONORABLE DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Washington, D.C. 20231

APPEAL BRIEF

IN SUPPORT OF APPELLANTS' APPEAL

TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicants (hereafter "Appellants") hereby submit this Brief in triplicate in support of their Appeal from a final decision by the Examiner in the above-captioned case. Appellants respectfully request consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the claims in the above-captioned patent application.

An oral hearing is not desired.

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
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WASHINGTON, D.C. 20231, ON: October 12, 2001
Date of Deposit

INTEL CORPORATION
Name of Assignee

SIGNATURE 10/12/01 DATE

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-27 are currently pending in the above-referenced patent application. Claims 1-27 were rejected in the Final Office Action mailed on May 2, 2001 and are the subject of this appeal. The Examiner confirmed his final rejection in an Advisory Action mailed on July 27, 2001.

Claims 1-27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. patent 5,442,474 by Huang et al.

IV. STATUS OF AMENDMENTS

To the best of Appellants' knowledge, no amendments have been filed subsequent to the Final Rejection.

A copy of all claims on appeal, namely claims 1-27 is attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

Simply stated and generally speaking, in one embodiment of Appellant's invention a method for routing encoded signals through a network is provided. Although the scope of Appellant's invention is not limited in this respect, the encoded signals are in a packet that comprises a header that may be received and decoded by a switch (e.g. switch 140 in FIG. 1.). At least a portion of the header may include encoded binary digital signals specifying a route through the network for the packet through the network. The switch may be able to determine the routing without decoding the header portion. More specifically, rather than decoding bits in a header that provides a switch information on how to route a packet to a destination port and then re-encoded those bits, Appellant's embodiment provides a technique where a bit pattern is chosen for the header so that when the bit pattern is encoded, it directly provides information regarding routing the packet through the network in its encoded form. (see page 10, lines 3-10 of Appellant's specification)

Therefore, in this particular embodiment of Appellant's invention, the encoded binary digital signals specify a route through the network without decoding. This may be accomplished using a look-up table in a route unit or router, for example, although the scope of Appellant's invention is not limited in scope in this respect. (see page 10, lines 10-13).

FIG. 2 provides an example of how a packet may be arranged in accordance with a particular embodiment of Appellant's invention. As shown, a packet may include a destination address as part of a header 310, a trailer 330 for use in cyclical redundancy checking, for example, and a payload 320. The payload may include the data or binary digital signals being transferred. (see page 8, lines 16-20, of Appellant's specification).

Simply stated, Appellants' claimed invention includes, as just one embodiment:

1. A method of routing a packet (e.g. packet shown in FIG. 2) of binary digital signals through a network, said method comprising:

receiving at a switch (e.g. switch 140) in said network the packet of binary digital signals as encoded binary digital signals including a bit pattern (e.g. bits in header

310) chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through the network in its encoded form; and

copying said bit pattern, at least for decoding.

VI. ISSUES PRESENTED

Whether claims 1-27 are unpatentable 35 U.S.C. § 102(b) as being anticipated by U.S. patent 5,442,474 by Huang et al.

VII. GROUPING OF CLAIMS

For the purposes of this appeal:

Claims 1-27 stand or fall together as Group I.

VIII. ARGUMENT

A. REJECTION OF CLAIMS 1-27 (GROUP I) UNDER 35 U.S.C. § 102(b) ON HUANG ET AL. IS IMPROPER. HUANG ET AL. DOES NOT EXPRESSLY OR INHERENTLY MEET CLAIM LIMITATIONS DIRECTED TO "A BIT PATTERN CHOSEN SO THAT WHEN THE BIT PATTERN IS ENCODED IT DIRECTLY PROVIDES INFORMATION REGARDING ROUTING THE PACKET THROUGH THE NETWORK".

The Examiner has rejected claims 1-27 under 35 U.S.C. §102(b) as being anticipated by Huang et al. (hereinafter "Huang"). As is well-established, for a document to anticipate a claim under 35 U.S.C. §102(b), the document must disclose all the elements and limitations of the claim. See, e.g., Scripps Clinic & Research Foundation v. Genentech, Inc., 18 USPQ2d 1001, 1010 (Fed. Cir. 1991). Therefore, if Huang does not meet even one element or limitation of claim 1, then a *prima facie* case of anticipation has not successfully been made.

Claim Group I

Claim 1 states:

1. A method of routing a packet of binary digital signals through a network, said method comprising:

receiving at a switch in said network the packet of binary digital signals as encoded binary digital signals including a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through the network in its encoded form; and

copying said bit pattern, at least for decoding.

It is respectfully asserted that a prima facie showing has not be established because Huang et al. fails to meet either expressly or inherently the limitation that the

encoded binary digital signals "directly provide information regarding routing the packet through the network."

Huang does not teach a header that directly provide information regarding routing

According to the Final Office Action, Huang et al. teaches a multiplexer 100 that encodes input data for sending binary signals to a switch 130. "The binary encoded signals includes [sic] a bit pattern (header bits) so that when the bit pattern is encoded it directly provides routing information (see col. 3, lines 47-55)." However, Appellants respectfully submit that the Final Office Action has mischaracterized the term "header bits" as bits that determine the destination of a packet of data, and consequently, has failed to establish a prima facie showing of anticipation.

Huang et al. specifically teaches that header bits are used only to indicate the beginning of each frame of data. More importantly, the header bits do not represent any encoded information that dictates the destination of the data. In particular, Huang et al. states: "Additionally, multiplexer 100 includes circuitry for providing a header signal indicating the beginning of each frame of multiplexed optical data signal." (column 2, lines 25-27).

Huang et al. teaches at column 4, lines 11-59, that Sagnac gates 141 and 142 are used to detect the unique header bit pattern H1 and H2 (shown in FIG. 2). Sagnac gate 141 is used to detect the occurrence of header bit H1 and then enable Sagnac switch 142 to detect the second header bit, H2. Header bits H1 and H2 are used to indicate the beginning of a data stream. Thus, header bits H1 and H2 do not contain any information, encoded or otherwise, that designates where the data is to be routed. Instead, header bits H1 and H2 are merely used to indicate the beginning of a frame of data. Consequently, because information explaining how to route the packet is contained elsewhere, the header bits cannot provide this information directly.

Even the Final Office Action admits that the header bits described in Huang et al. do not themselves contain the information used to route the packet. Instead, the header bits taught in Huang et al. only indicate the start of the routing bits. Thus, the header bits cannot directly provide information on how to route the packet through the network.

The Examiner has ignored language recited in the claims

In the Advisory Action, the Examiner stated: "Huang teaches the use of a special header bit coding so that the header bits can be readily detected (see col. 3, lines 47-53). Header bits provide information regarding where/when routing bits appear (i.e. routing information)."

However, the Examiner's statement in the Advisory Action is incomplete and should be afforded no weight. The Examiner has again failed to explain how the header bits in Huang directly provide routing information. Instead, the Examiner argues that routing information can be located outside of the header once the location of the header is detected. The Examiner's comments are not relevant because this is not what is recited in Appellant's claim 1.

According to the Final Office Action the header bits appear at the beginning of the packet which is in front of the routing bits; implying that detection of the header bits means that the routing bits will follow. (see Final Office Action page 2). Using this as its basis, the Final Office Action then goes on to conclude that "... the header bits provide the information regarding where/when the routing bits are supposed to appear/arrive" and that the routing bits are used to route the packet through the network.

However, Appellants respectfully point out that the conclusion made in the Final Office Action fails to address the term "**directly**" as recited in claim 1. Claim 1 recites, among other things, that "when the bit pattern is encoded it **directly** provides information regarding routing the packet through the network in its encoded form." (emphasis added) In contrast, the header bits described by Huang do not contain any information regarding the routing of the packet. Since the header bits themselves do not contain any routing information, it is not possible for the header bits to directly provide information regarding the information.

The Examiner's arguments and statement in the Advisory Action improperly ignores the term "directly" as it is recited in the claim. Consequently, the Examiner has failed to establish that each feature or limitation of claim 1 is anticipated by Huang. Accordingly, the rejection under 35 USC §102(b) must be improper.

Accordingly, the Final Office Action has failed to establish a prima facie showing of how Huang et al. anticipates every element and limitation of Appellants' claim 1.

Therefore, Appellants respectfully traverse the rejection. Since claims 2-9 depend from independent claim 1, they are not anticipated by Huang et al. for at least the same reason.

With regard to independent claims 10, 17, 22, and 25, Appellants would like to kindly point out that each independent claim also recites, among other things, "... that when the bit pattern is encoded it directly provides information regarding routing of the packet... ." As pointed out above, the header bits disclosed by Huang et al. do not contain any information regarding the routing of the packet as suggested by the Final Office Action. Accordingly, the Final Office Action has failed to establish a prima facie showing of anticipation for claims 10, 17, 22, and 25. Since claims 11-16, 18-21, 23-34, and 26-27 depend from claim 10, 17, 22, and 25, respectively, they are not anticipated for at least the same reason.

Additional arguments to distinguish the cited patent from claims 1-27 could have been made, but it is believed that the foregoing discussion is sufficient to overcome the Examiner's rejection.

IX. CONCLUSION

Appellants respectfully submit that all the pending claims in this patent application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims and objected claim 7.

This brief is submitted in triplicate, along with a check for $320.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overcharges to Deposit Account No. 02-2666.

Respectfully submitted,

Date: 10-12-01

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X. APPENDIX A: CLAIMS ON APPEAL

1. A method of routing a packet of binary digital signals through a network, said method comprising:

receiving at a switch in said network the packet of binary digital signals as encoded binary digital signals including a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through the network in its encoded form; and

copying said bit pattern, at least for decoding.

2. The method of claim 1, and further comprising a step of decoding the copied encoded binary digital signals.

3. The method of claim 2, wherein the step of receiving the packet of binary digital signals comprises receiving the packet serially; and further comprising a step of deserializing the decoded binary digital signal.

4. The method of claim 3, and further comprising a step of translating the deserialized and decoded binary digital signals.

5. The method of claim 4, and further comprising a step of routing the received packet of binary digital signals in accordance with the translated binary digital signals.

6. The method of claim 5, wherein the step of routing comprises routing the packet of binary digital signals to another switch in the network.

7. The method of claim 5, wherein the step of routing comprises routing the packet of binary digital signals to its destination in the network.

8. The method of claim 1, wherein said encoded binary digital signals used to route the packet through the network comprise an encoded destination address.

9. The method of claim 1, wherein said encoded binary digital signals used to route the packet through the network comprise encoded binary digital signals specifying a route through the network if desired.

10. An integrated circuit comprising: a switch adapted to receive a packet of binary digital signals as encoded binary digital signals including a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through the network in its encoded form;
said switch being further adapted to copy the encoded binary digital signals including the bit pattern, at least for decoding.

11. The integrated circuit of claim 10, wherein said switch is further adapted to serially receive said packet and to serially copy the encoded binary digital signals used to route the packet through the network.

12. The integrated circuit of claim 11, wherein said switch is further adapted to decode and deserialize of the copied encoded binary digital signals used to route the packet through the network.

13. The integrated circuit of claim 12, wherein said switch is further adapted to translate the decoded and deserialized binary digital signals.

14. The integrated circuit of claim 13. wherein said switch is coupled in the network, said switch being adapted to route the received packet of binary digital signals in accordance with the translated binary digital signals.

15. The integrated circuit of claim 10, wherein the encoded binary digital signals used to route the packet through the network comprise an encoded destination address.

16. The integrated circuit of claim 10, wherein the encoded binary digital signals used to route the packet through the network comprise encoded binary digital signals specifying a route through the network if decoded.

17. A method of routing a packet of binary digital signals through a network, said method comprising:

receiving at a switch in the network the packet of binary digital signals as encoded binary digital signals including a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through the network in its encoded form without decoding.

18. The method of claim 17, wherein said encoded binary digital signals specifying a route through the network without decoding comprise a portion of the header of the packet of binary digital signals.

19. The method of claim 17, and further comprising a step of: routing the packet of binary digital signals in accordance with the encoded binary digital signals specifying a route through said network without decoding.

20. The method of claim 19, wherein the step of routing comprises routing the packet of binary digital signals to another switch in the network.

21. The method of claim 19, wherein the step of routing comprises routing the packet of binary digital signals to a destination in the network.

22. An integrated circuit to receive a packet of binary digital signals, the packet of binary digital signals including a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through a network in its encoded form without encoding.

23. The integrated circuit of claim 22, wherein said encoded binary digital signals comprise a portion of the header of the packet of binary digital signals.

24. The integrated circuit of claim 23, wherein said switch is coupled in the network, said switch being adapted to route the packet of binary digital signals in accordance with the encoded binary digital signals specifying a route through the network without decoding.

25. An integrated circuit comprising: a route unit adapted to produce binary digital signals to be included in a packet of binary digital signals that after encoding includes a bit pattern chosen so that when the bit pattern is encoded it directly provides information regarding routing the packet through a network in its encoded form without decoding.

26. The integrated circuit of claim 25, wherein said route unit is embodied in a network interface component (NIC).

27. The integrated circuit of claim 26, wherein said NIC is coupled to a switch, said switch being adapted to route the packet of binary digital signals through the network in accordance with the encoded binary digital signals specifying a route through the network without decoding.

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/124,640
Filing Date	July 29, 1998
First Named Inventor	Jie Ni
Group Art Unit	2664
Examiner Name	P. Tran
Attorney Docket Number	42390P6190

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Total Number of Pages in This Submission: 48

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- ☐ To Convert a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Small Entity Statement
- ☐ Request for Refund
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Additional Enclosure(s) *(please identify below):*

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Donna Jo Coningsby, Reg. No. 41,684 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Donna Jo Coningsby
Date	October 12, 2001

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FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 310.00

Complete if Known	
Application No.	09/124,640
Filing Date	July 29, 1998
First Named Inventor	Jie Ni
Examiner Name	P. Tran
Group/Art Unit	2664
Attorney Docket Number	42390P6190

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to credit any overpayments to:

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

☒ Charge Any Additional Fee(s) Required Under 37 CFR §§ 1.16,1.17, 1.18 and 1.20.

☐ Applicant claims small entity status. See 37 CFR 1.27.

2. ☒ **Payment Enclosed:**

☒ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	Fee Paid
Total Claims		-		=	X	=	
Independent Claims		-		=	X	=	
Multiple Dependent						=	

**or number previously paid, if greater, For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	260	204	140	Multiple Dependent claim, if not paid
109	84	209	42	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	*Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	*Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	400	216	200	Extension for response within second month	
117	920	217	460	Extension for response within third month	
118	1,440	218	720	Extension for response within fourth month	
128	1,960	228	980	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	310.00
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	130	123	130	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

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Signature	Donna Jo Coningsby			Date	10/12/01

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